Monolithic MESFET Distributed Baluns Based on the Distributed Amplifier Gate-Line Termination Technique

Atiqul H. Baree, *Student Member, IEEE,* and Ian D. Robertson

***Abstract*— The principles of the distributed amplifier are applied to realize wide-band monolithic distributed baluns. The technique reported here is based on using the gate-line "termination" of a distributed amplifier topology as the noninverting output and the inherent phase inversion property of the metal-semiconductor field-effect transistor (MESFET) to provide the antiphase output from the drain-line. Closed-form expressions are derived for the two output voltage signals and their respective power gains. The theoretical performance of the balun is then examined as a function of the important MESFET parameters and other circuit parameters. Some practical design considerations are given followed by the measured results of two monolithic prototypes. The first is a basic two-section balun, while the second employs a four-section balun with a three-stage positive gain slope preamplifier to compensate for the increase in gate-line loss with frequency. Balun operation over 0.5–20 GHz and 0.5–12 GHz has been demonstrated for the two-section and four-section balun, respectively.**

***Index Terms*—Balun, distributed amplifier, MESFET, MMIC.**

I. Introduction

BALUNS are required in key microwave components such as balanced mixers, push-pull amplifiers, multipliers, and phase shifters. The need for broad-band monolithic baluns is becoming ever greater as monolithic microwave integrated circuit (MMIC) technology advances. A number of different methods have been employed to realize MMIC baluns. These include: 1) planar transformer techniques [1], [2]; 2) Marchand baluns using multi-layer techniques [3]; 3) coplanar waveguide (CPW) to slotline transition baluns [4], [5]; and recently 4) a technique using simple RF reflection and coupling principles [6]. However, since all these techniques use transmission line concepts, they have a bandwidth limitation at low frequency because on MMIC's they cannot be made large enough for good low frequency operation.

For MMIC applications, active baluns using the traveling wave-matching technique have the potential of providing good wide-band performance without consuming too much expensive circuit area. The traveling wave technique for baluns has been demonstrated by Pavio *et al.* [7]; however, their technique employs pairs of FET's connected in a common-gate common-source configuration and so has an ultimate bandwidth limitation because the common-gate FET's cause very high attenuation along the input line.

In this paper, an alternative traveling wave technique based on the principles of the distributed amplifier [8]–[11] is reported. In the distributed amplifier, the gain-bandwidth product is increased by paralleling several FET's without paralleling their input or output capacitances, thus achieving operation over extremely wide bandwidths. The basis of this reported technique is to exploit the distributed amplifier topology and use the normally terminated gate-line as a noninverting balun output. The antiphase output is provided by the phase-inverting properties of the MESFET.

The design of the MESFET distributed balun involves a careful choice of parameters such as the device, the number of devices, and the parameters of the artificial transmission lines. Starting with a theoretical analysis of the structure to derive the power and phase relationships between the input and outputs, the performance of the balun is then investigated as a function of the important MESFET and circuit parameters. We then provide some general design guidelines, followed by a discussion on the measured performance of two monolithic prototypes.

II. Circuit Description and Analysis

Fig. 1 shows the schematic representation of the distributed balun. The gate and drain impedances of the FET's are absorbed into lossy artificial transmission lines, designated as the gate and drain transmission lines, L_g and L_d, respectively. The inductor connecting the MESFET to the drain output transmission lines is designated L_{dd} and assumed zero to simplify the analysis. Coupling between the two transmission lines is provided by the device transconductance g_m.

We will assume the simple unilateral MESFET model shown in Fig. 2. C_{gs} is the gate-to-channel capacitance, r_g is the gate input resistance, and C_{ds} and R_{ds} are the drain-to-source capacitance and resistance, respectively. With this common-source MESFET model, the equivalent gate and drain transmission lines are shown in Fig. 3. It is clear that a wave from the generator E_s propagates down the gate-line with a phase constant β_g per section and appears finally across the gate load Z_{og}. As the signal travels down the gate-line, the voltage across each gate capacitor V_{Cgs} feeds a current

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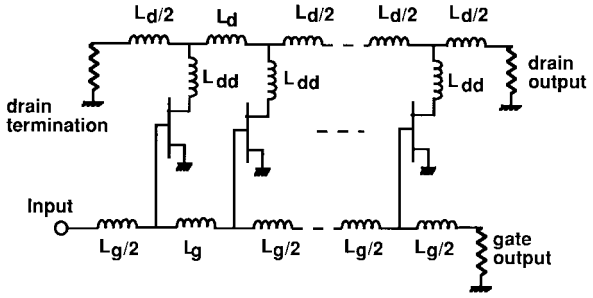


Fig. 1. Schematic of the distributed active balun.

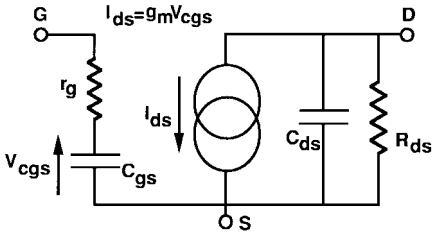
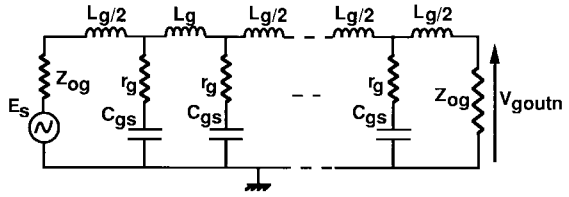
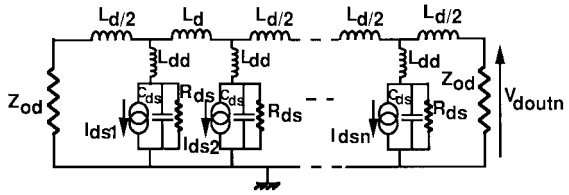


Fig. 2. Simplified MESFET model.



(a)

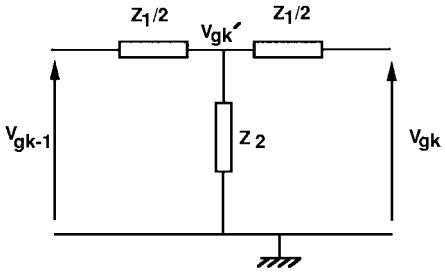


(b)

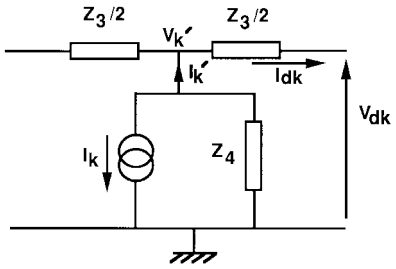
Fig. 3. (a) Equivalent gate transmission line. (b) Equivalent drain transmission line.

$g_m V_{Cgs}$ into the drain-line, the phase of which is determined by the MESFET and circuit parameter values. The current from each generator flows in both directions with phase constant β_d per section. Reverse traveling waves are absorbed in the reverse drain-line termination, while by proper selection of the MESFET and circuit parameters the phase velocities on the gate- and drain-lines can be made to be equal and so add in the forward direction as they arrive at the drain load Z_{od}. Balun operation is achieved if the two signals appearing across the gate and drain loads are made equal and antiphase.

It is clear from Fig. 3 that the distributed balun is composed of two constant-k gate- and drain-lines (as shown in Fig. 4) which have different cutoff frequencies and attenuation characteristics. Considering the gate-line first, it can easily be shown that the total voltage appearing across the gate-line load Z_{og}



(a)



(b)

Fig. 4. Constant-k (a) gate-line section and (b) drain-line section.

for an n section balun is given by

$$V_{goutn} = \frac{Z_{og}}{Z_{og} + \frac{Z_1}{2}} \Delta_{Zpp} \Delta_{Zp} E_s e^{-(n-1)\gamma_g} \tag{1}$$

where γ_g is the propagation function per section, Z_{og} is also the image impedance and

$$\Delta_{Zp} = \frac{Z_p}{Z_p + \frac{Z_1}{2}} \tag{2}$$

$$\Delta_{Zpp} = \frac{Z_p + \frac{Z_1}{2}}{Z_p + \frac{Z_1}{2} + Z_{og}} \tag{3}$$

with

$$Z_p = \frac{Z_2\left(Z_{og} + \frac{Z_1}{2}\right)}{Z_{og} + \frac{Z_1}{2} + Z_2}. \tag{4}$$

Considering the constant-k drain-line section of Fig. 4(b), it is shown in the Appendix that

$$I_{dk} = \Delta_d I_k \tag{5}$$

where

$$\Delta_d = \frac{Z_4}{2Z_4 + Z_3/2 + Z_{od}}. \tag{6}$$

$I_1, I_2, \cdots, I_n$ are the current generators given by $I_1 = g_m V C_{gs1}, I_2 = g_m V_{Cgs2}, \cdots, I_n = g_m V_{Cgsn}$. Then, since superposition applies, the total forward current in the drain load Z_{od} is given by

$$I_{doutn} = I_{d1} e^{-(n-1)\gamma_d} + I_{d2} e^{-(n-2)\gamma_d} + I_{d3} e^{-(n-3)\gamma_d} + \cdots I_{dn}. \tag{7}$$

Thus, the total voltage across Z_{od} can be shown to be given by

$$V_{doutn} = -g_m Z_{od} \Delta_d \Delta_{Zp} \Delta_{Zpp} \Delta_{ZCgs} E_s \cdot \sum_{r=1}^{n} e^{\{-(n-r)\gamma_d - (r-1)\gamma_g\}} \quad (8)$$

where

$$\Delta_{Z_{Cgs}} = \frac{1}{1 + j\omega C_{gs} r_g} \quad (9)$$

since the input power to the balun P_i and the power P_o delivered to a load Z_L with current I flowing through it are given, respectively, by

$$P_i = \frac{|V_{go}|^2}{2|Z_{og}|^2} \mathrm{Re}[Z_{og}] \quad (10)$$

and

$$P_o = \tfrac{1}{2}|I|^2 \mathrm{Re}[Z_L]. \quad (11)$$

Then the available power gain of the gate-line and forward drain-line can be shown to be given, respectively, by

$$P_{gg} = \left| \frac{Z_{og}}{Z_{og} + \frac{Z_1}{2}} \Delta_{Zp} e^{-(n-1)\gamma_g} \right|^2 \quad (12)$$

$$P_{gf} = g_m \left| \Delta_d \Delta_{Zp} \Delta_{Z_{Cgs}} \sum_{r=1}^{n} e^{\{-(n-r)\gamma_d - (r-1)\gamma_g\}} \right|^2. \quad (13)$$

III. Examination of Power and Phase Response

The derived analysis allows one to directly calculate the phase and power gain response of the balun and thus examine the effect of the MESFET and circuit parameters on the balun response. To demonstrate the validity of the analysis and the effects of the more significant parameters, a basic transistor model with $C_{gs} = 0.14$ pF, $r_g = 13\ \Omega$, $C_{ds} = 0.02$ pF, $g_m = 0.018$ S and $R_{ds} = 580\ \Omega$ is assumed, although a practical design would use modeled element values from a measured set of device parameters. It should be noted that at this stage, the primary objective is only to examine the effects of the more significant parameters on the circuit response and no attempt is made to design the circuit for optimum performance.

By looking at the power response of the distributed balun first, one would intuitively expect the gate- and drain-line attenuations to be the critical factors controlling the frequency response of the distributed balun. For the distributed amplifier, Beyer *et al.* [9] have investigated the gate and drain-line attenuations as a function of the gate-circuit, drain-circuit, and transmission line cutoff frequencies, and their results have shown that the gate-line attenuation increases steadily with frequency and vanishes to zero in the low frequency limit; in contrast, drain-line attenuation is more or less constant with frequency. Since the target gain of the balun is unity, the FET gate widths are small and the drain-line attenuation can easily be compensated for by increasing the gate widths slightly (higher g_m); however, the gate-line loss remains as the limiting factor in the performance of the balun. Fig. 5 shows the balun power responses calculated using the derived expressions for the gate- and drain-line power gains (12) and (13). It shows that a low value of r_g is crucial to maintaining a broad-band performance without high insertion loss. Fig. 5(b) shows that it is difficult to obtain flat drain-line gain at low frequencies. This is found to be due to the FET output resistance R_{ds}. By using a device with high R_{ds} (3 kΩ) the low frequency gain can be increased and an extremely flat response can be achieved as shown in Fig. 6. Of course, such a high R_{ds} value may not be practical, but in fact this poor drain-line gain flatness is mainly an artifact of the use of image terminations in the analysis and is not found to be a problem in practice as we shall see later.

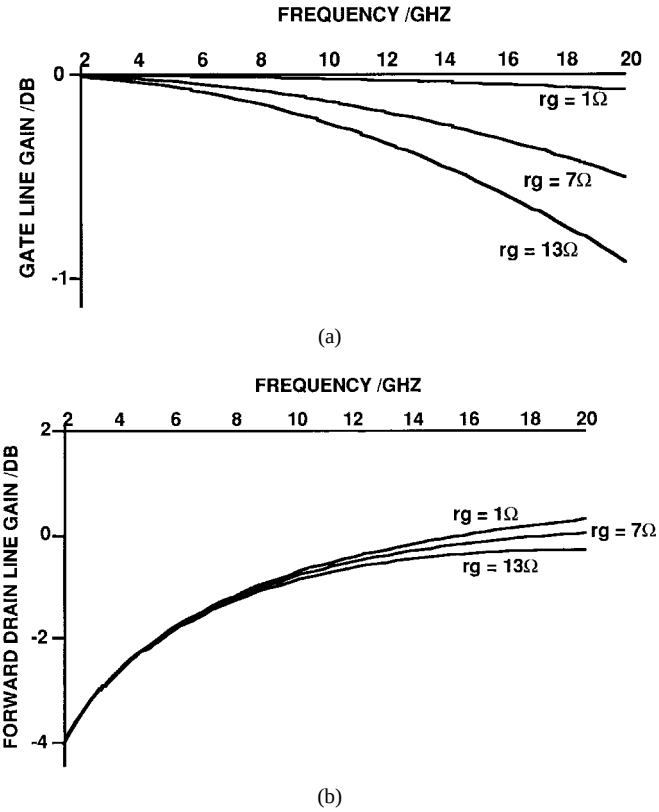


Fig. 5. Effect of r_g on (a) Gate-line gain. (b) Forward drain-line gain for $n = 2$, $C_{gs} = 0.14$ pF, $C_{ds} = 0.02$ pF; $Rds = 580\ \Omega$, $gm = 0.018S$, $L_g = 0.1$ nH, $Ld = 0.7$ nH.

The effect of increasing the number of sections, n, of the distributed balun is to increase the maximum forward drain-line gain. In order to maintain unity gain, the FET gate widths must therefore be decreased (or the bias current reduced) in order to lower g_m. The result of adding more sections and lowering the gate widths is that the gate-line attenuation increases significantly. As a result, there are some difficult tradeoffs to be addressed when considering the optimum number of sections. Adding more sections could improve the input and output matching, for example, but one would need to compensate for the increased gate-line loss when using a larger number of sections. The practical means of compensating for this adverse effect are discussed in the next section. The phase response is also a strong function of the number of sections because any residual difference between the gate- and drain-

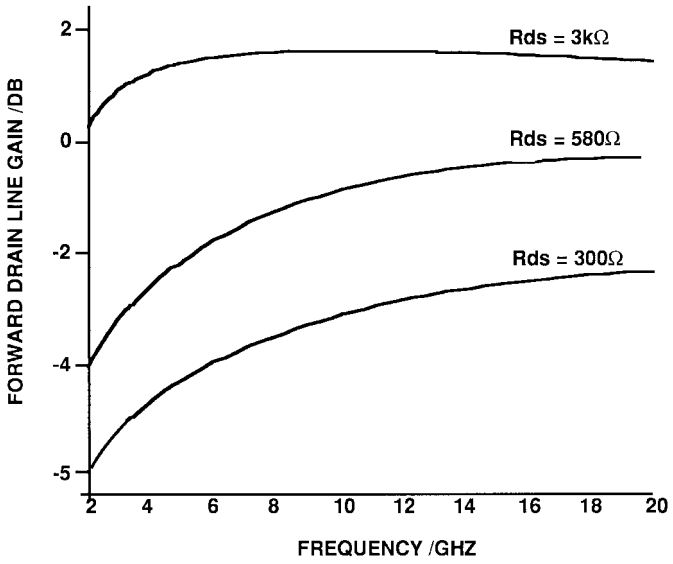


Fig. 6. Effect of R_{ds} on forward drain-line gain for $n = 2$, $r_g = 13\ \Omega$; $C_{gs} = 0.14$ pF, $C_{ds} = 0.02$ pF, $gm = 0.018$ S, $Lg = 0.1$ nH, $Ld = 0.7$ nH.

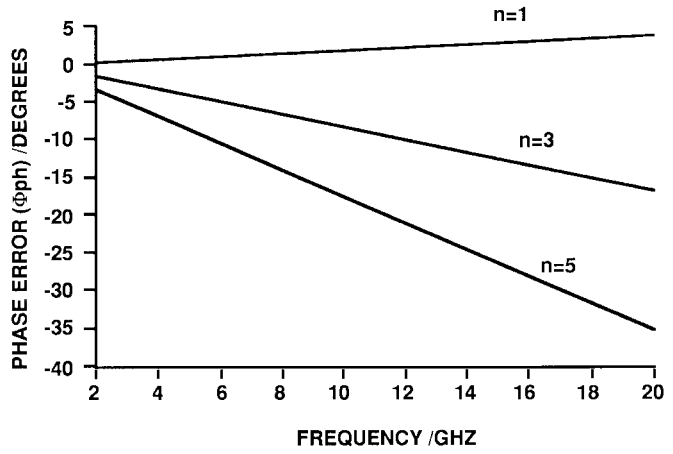


Fig. 7. Effect of n on phase error for $r_g = 13\ \Omega$, $C_{gs} = 0.14$ pF, $C_{ds} = 0.02_{\mathrm{pF}}$, $R_{ds} = 580\ \Omega$, $gm = 0.018$ S, $L_g = 0.1$ nH, $Ld = 0.7$ nH.

line propagation constants becomes more serious when the signals travel along more sections. Fig. 7 shows the change of Φ_{ph} (i.e., the phase error defined as the phase difference from 180° between the forward drain and gate outputs) as the number of sections, n, is changed. It is clear that the addition of more sections deteriorates the phase performance of the balun. Since an optimum number of sections is needed for good amplitude response, practical means of compensating for the increase in Φ_{ph} with n is discussed in the next section.

IV. Practical Design Considerations

An assumption inherent in this analysis is that the gate and drain transmission lines be terminated with their image impedances. Since the image impedances are a function of frequency and approaches infinity at cutoff, there is no physical combination of elements that can provide a proper termination at all frequencies. Distributed matching networks such as the constant-k m-derived network, however, can be

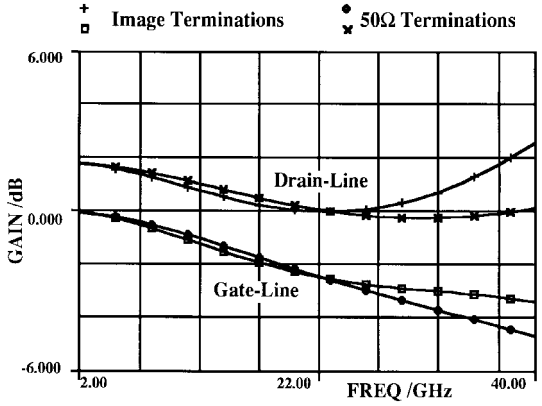


Fig. 8. Gain comparisons using practical m-derived image impedance terminations and 50 Ω terminations.

used to terminate the transmission lines through an operating frequency limit of $0.8f_c$ [12] (f_c is the cutoff frequency of the transmission lines) but these can only be realized using lumped components and can consume valuable circuit area. The GEC–Marconi materials technology (GMMT) process MESFET's, which are the MESFET's employed in the designs considered in this paper, have a maximum operational bandwidth of up to only 20 GHz while the f_c of the lines is much higher (about 85 GHz for the parameters set above). Thus, it is the MESFET parameters that set the upper limit of operation and one needs to consider whether the use of the m-derived matching networks are necessary. It should be possible to use simple 50 Ω terminations and achieve the same results as for the m-derived image terminations. To demonstrate this, we show in Fig. 8 a comparison of the gate- and drain-line gains using a practical constant-k m-derived image terminating network (with $m = 0.6$) and 50 Ω terminations, both using small-signal foundry models for the devices. It is clear that close agreement is obtained over the operational bandwidth of the MESFET while for frequencies exceeding this the difference becomes far greater. A similar comparison of the phase error (Fig. 9) shows the agreement to again be very close only over the operational bandwidth of the MESFET. The results suggest that, for the devices in consideration, one can replace the image termination impedances with 50 Ω terminations and we have taken advantage of this property to design the baluns using 50 Ω terminations.

The design of the distributed balun involves the design of small-valued lumped inductors which are best realized in MMIC's using short lengths of high impedance microstrip lines. For short lengths ($l < \lambda_g/7$) the inductance L and its associated end capacitances C are given, respectively, by [13]

$$L \approx \frac{Z_0}{2\pi f} \sin\left(\frac{2\pi l}{\lambda_g}\right) \tag{14}$$

and

$$C \approx \frac{1}{2\pi f Z_0} \tan\left(\frac{\pi l}{\lambda_g}\right) \tag{15}$$

where Z_0 is the characteristic impedance of the microstrip line, f is the frequency, and λ_g is the wavelength in the microstrip line. With computer-aided design, the end capacitances can easily be absorbed into the gate- and drain-lines

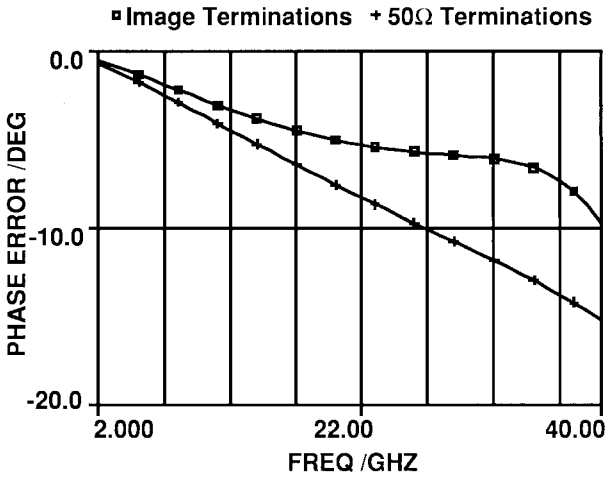
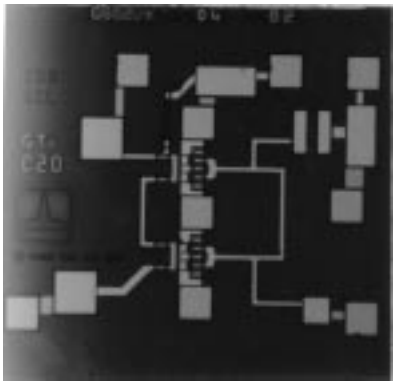


Fig. 9. Phase error comparisons using practical m-derived image impedance terminations and 50 Ω terminations.

by incorporating them in the design of the transmission lines. Ideally, a narrow track with high Z_0 is needed to achieve high inductance with low parasitic capacitance. In practice, however, the minimum track width is determined by fabrication limits (as the width may be too small to be realizable), the excessive attenuation of narrow tracks, and the dc current-carrying capacities as there will be excessive electromigration of the metal as a result of the high current densities. The upper and lower limits of l will also be restricted by geometrical considerations in the layout.

It is important in the balun design to have equal magnitude and antiphase signals at the two gate and drain outputs. It is apparent from the simulations that the amplitude difference increases with frequency and also increases as the number of sections, n, is increased. If one is to employ the optimum number of sections to obtain a broadband balun, some form of compensation is required to maintain equal gate and drain power outputs. Resistive attenuation on the drain-line would lower the drain-line gain and so can potentially be used to equalize for the two outputs. This does, however, have the detrimental effect of a) poorer noise figure; b) more dc power consumption; and c) reduction in the overall gain-bandwidth product. A much simpler and better approach is to reduce g_m accordingly as n is increased (i.e, use smaller size FET's). This alone, however, does not alleviate the problem of gate- and drain-line losses increasing with frequency. It is the gate-line loss that predominantly affects the gain in both gate- and drain-lines, and by compensating for the gain-drop-off in the gate-line with frequency, one can recover the gain flatness for both gate- and drain-line outputs. A gate-line preamplifier designed with a positive gain slope is an effective means of compensating for the gain drop-off with frequency and is the preferred approach to compensation since this has the added advantage of better noise figure and an inherent reverse isolation (i.e., output to input isolation) due to the S_{12} of the preamplifier FET's.

With regard to the phase error between the gate and drain outputs, we know that this increases with frequency and also with n. To compensate for this, one can use a section



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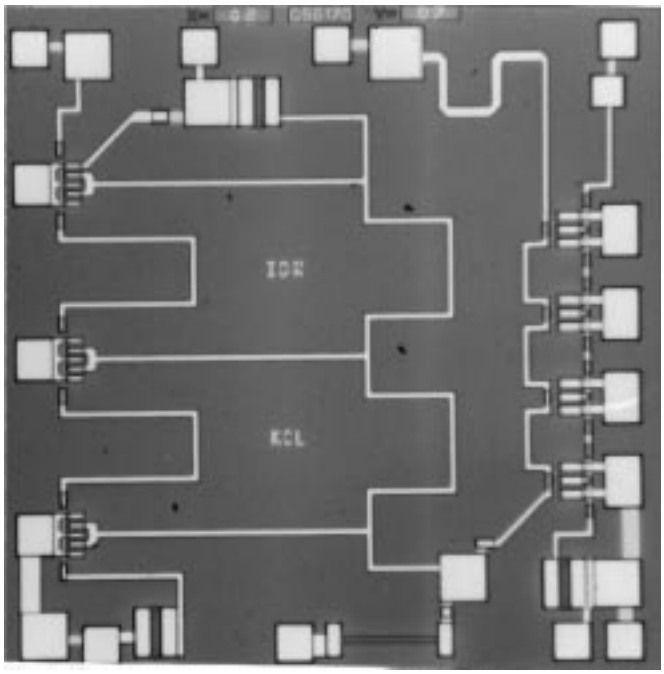


(b)

Fig. 10. Photomicrographs of (a) two-section balun with no gate-line loss compensation and (b) four-section balun with three-section positive gain slope preamplifier to compensate for the increase in gate-line loss with frequency.

of microstrip transmission line at the gate-line output. The microstrip line has the effect of shifting the gate signal phase, more so at high frequencies. Thus, for a given number of sections, the microstrip line length can be optimized to shift the gate-line phase by the necessary amount to obtain the required 180° phase difference (0° phase error).

V. Measured Performance

We present in this section the performance of two monolithic distributed baluns; the first employs only two sections with no gate-line preamplifier, while the second employs a four-section balun with a three-section gain-error compensation preamplifier. Both baluns utilize an optimized length of microstrip line at the gate-line output for phase-error compensation and use 50 Ω terminations. The two-section balun was fabricated using the GMMT F20 (Caswell) Foundry process, which provides MESFET operation up to 20 GHz, while the four-section balun was fabricated using the GMMT F14 Foundry process, which

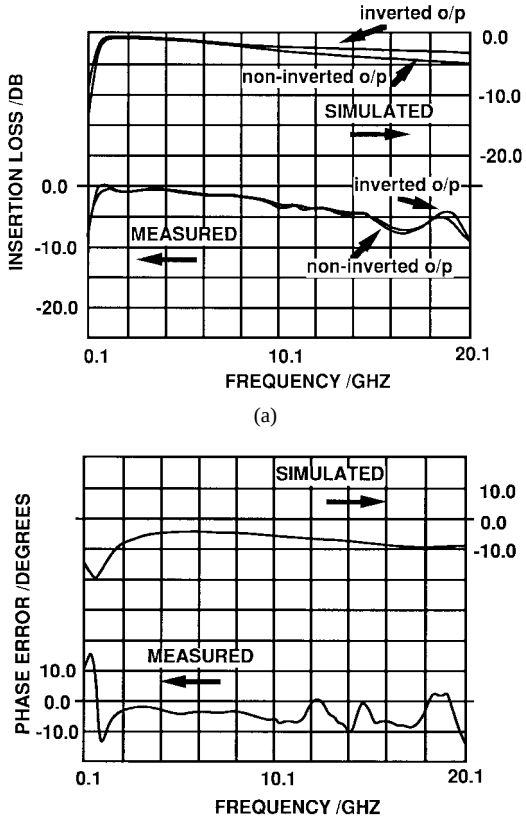


Fig. 11. Measured and simulated response of two-section balun. (a) Insertion loss. (b) Phase error.

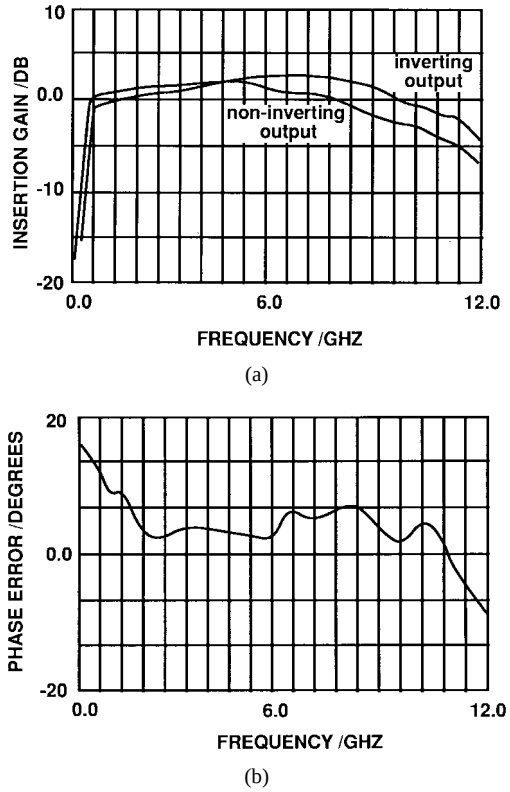


Fig. 12. Measured response of four-section balun. (a) Insertion loss. (b) Phase error.

provides operation only up to 14 GHz. It was necessary to change processes as the circuits were on shared university multiproject wafers and were not fabricated at the same time.

In brief, both F14 and F20 processes are based upon direct ion-implantation into LEC semi-insulating GaA's with Ti/Pt/Au gate metallizations. A two-level metallization scheme is employed and the metallization levels are separated by a composite SiNi and polyimide dielectric layer substrates. The differences in the two processes are that process F20 uses 0.5 μm gate lengths and allows through GaA's via-holes; the F14 process allows no via-holes and uses 0.7 m MESFET gate lengths. The final die thickness is 200 μm for both processes. Photomicrographs of the two chips are shown in Fig. 10.

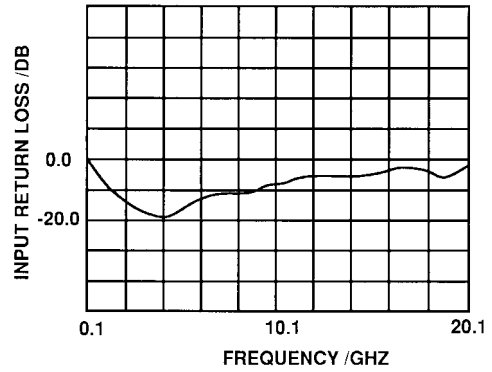
The measured power gain response and phase error for the two-section balun is shown in Fig. 11. As a comparison, the simulated response for the ideal case using 50 Ω terminations is included in the same plot. The measured response shows ripples and is more lossy at high frequencies due to effects of the nonideal test fixture. Fig. 12 shows the measured response of the four-section balun. It can be seen that the maximum phase error is 10° over the operational bandwidth of both chips. We notice the significant improvement in the phase error of this technique over the alternate traveling wave technique presented in [7]. In [7], a phase error of $0\pm 35°$ was measured over 2–18 GHz.

For the two-section balun, we observe that although the insertion loss in the gate-line and drain-lines are almost identical over the operational bandwidth, this drops off at high frequencies due to r_g. The second chip, which includes the positive gain slope preamplifier, compensates for the gain drop-off and exhibits a very flat response. If the F20 process was used to fabricate this second chip, very flat operation up to 20 GHz would have been achieved. It must be said that the increase in performance of the four-section balun is at the expense of increased power consumption since more FET's are employed in the design. The power consumptions are approximately 100 mW and 350 mW for the two-section and four-section design, respectively.

The measured port matches for the two-section and four-section baluns are shown in Figs. 13 and 14, respectively, while the noise figure measurements are shown in Fig. 15 for the two-section balun only. The noise figure at the gate-line output (noninverted) is approximately equal to the gate-line loss, as there is little contribution to the noise figure from the FET's. The noise figure at the drain-line output is expected to be much better for the four-section balun because of the pre-amplifier at the input.

VI. Conclusion

We have presented in this paper the theoretical analysis and practical design considerations of monolithic MESFET distributed baluns based on the distributed amplifier gate-line termination technique. Having derived closed-form expressions for the two output signals and their respective power gains, simulations have been performed to show the effect of MESFET and circuit parameters on the theoretical performance of the balun. The most critical factor in determining the



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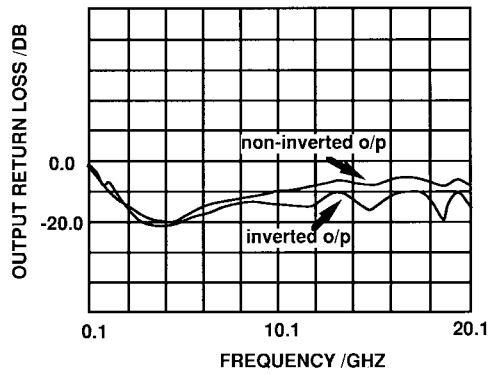
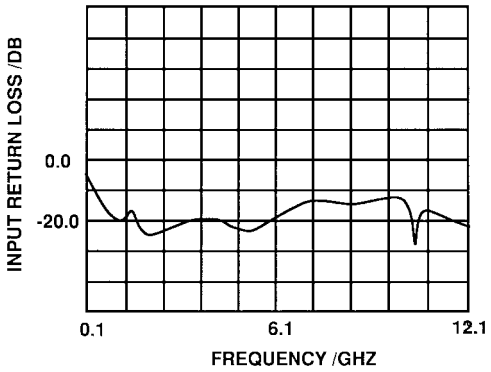
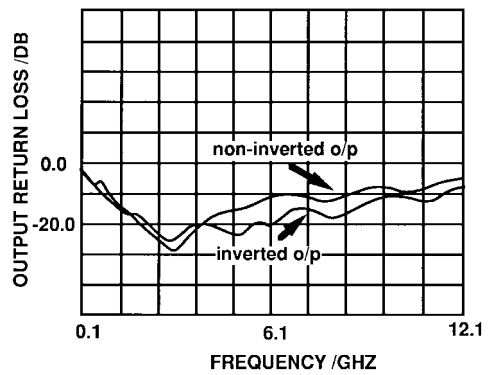


(b)

Fig. 13. Measured return loss of two-section balun. (a) Input. (b) Output.



(a)



(b)

Fig. 14. Measured return loss of four-section balun. (a) Input. (b) Output.

gain response of the balun is the transmission-line attenuation, with the gate-line typically being the dominant contributor due to high parasitic r_g. Low noise high electron mobility transistors (HEMT) devices have a much lower r_g, and so with the use of these devices one can expect very flat operation over much greater bandwidths.

The measured results of two monolithic prototypes have been presented and a comparison is made with the simulated results for the two-section balun, with close agreement obtained. Successful balun operation over 0.5–20 GHz has been demonstrated for the two-section balun. A four-section design has been realized with a positive gain-slope preamplifer incorporated to compensate for the gate-line loss and provide a flat response; operation up to 12 GHz has been demonstrated for this four-section balun. Both baluns described here have utilized identical balun sections. The use of nonidentical sections would allow greater flexibility in the design procedure. In particular, the gate and drain transmission line cutoff frequencies can be optimized more flexibly to compensate for the gate-line loss. Also the phase error can be corrected at the individual stages, rather than using a single length of microstrip line at the gate-line output.

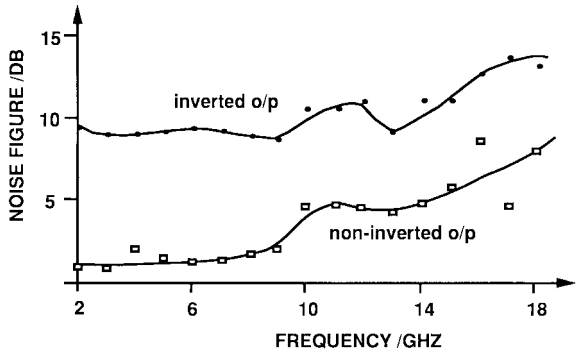


Fig. 15. Measured noise figure of two-section balun.

APPENDIX

Consider the kth drain-line section shown in Fig. 4(b). This can be transformed to its Thevenin equivalent form as shown in Fig. 16, where

$$I_k = I'_k - \frac{V'_k}{Z_4}. \tag{A1}$$

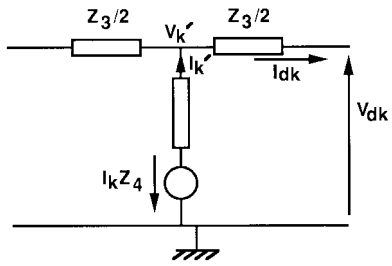


Fig. 16. Thevenin equivalent of the drain-line section.

It is clear from Fig. 16 that

$$I_{dk} = \frac{I'_k}{2} \tag{A2}$$

and also

$$I_{dk} = \frac{V_{dk} - V'_k}{\frac{Z_3}{2}} \tag{A3}$$

$$V_{dk} = \frac{Z_{od}}{Z_{od} + \frac{Z_3}{2}} V'_k. \tag{A4}$$

Rearranging (A1) for I'_k and substituting into (A2) yields

$$I_{dk} = \frac{I_k}{2} + \frac{V'_k}{2Z_4}. \tag{A5}$$

Rearranging (A3) in terms of V'_k, and substituting (A4) in the resulting expression and manipulating terms yields

$$V'_k = \frac{-(2Zod + Z3)}{2} I_{dk}. \tag{A6}$$

Substituting (A6) into (A5) and manipulating terms yields

$$I_{dk} = \Delta_d I_k \tag{A7}$$

where

$$\Delta_d = \frac{Z_4}{2Z_4 + \frac{Z_3}{2} + Z_{od}}. \tag{A8}$$

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